Conference Report:
The 11th Swedish System-on-Chip Conference

The 11th Swedish System-on-Chip Conference (SSoCC'11) was arranged May 2-3 2011 in Varberg in the western part of Sweden about 70 km south of Gothenburg on what some people may refer to as the "front side of Sweden" (which of course depends on your perspective!).

The conference was organized by the Swedish Chapter of the IEEE Solid-State Circuits Society (SSCS), with local support from the departments of Microtechnology and Nanoscience (MC2), and Computer Science and Engineering (CSE) at Chalmers University of Technology.

First held in 2001, and since 2006 organized by the Swedish SSCS, this has become the annual conference where the major part of the university researchers and PhD students in the analog/RF and digital circuit design areas in Sweden meet, enjoy and network. This year, the conference brought together 80 participants, and 47 papers were presented.

The local arrangements rotate between four large universities in Sweden and this year's conference was arranged by Chalmers University of Technology, Gothenburg. Chalmers was founded in 1829 and is named after William Chalmers who donated a large sum of money for a craft-school for poor children. Today, Chalmers is a well-reputable technical university with around 11,000 students and 1,100 Ph.D. students in different technical areas. Chalmers has a strong history in electronic devices and microwaves, and there are many local companies focused on applications of microwave technology. Besides large companies such as Ericsson AB and Ruag Space AB, the region also accommodates several successful spin-offs from Chalmers in the electronics area.

The conference venue Varbergs Kurort is very beautifully situated at the sea, a short distance from Varberg city center. The facility formerly known as Apelviken Coastal Sanatorium has a colorful history as the largest sanatorium in Scandinavia treating tuberculosis during a time when the vaccine was not as available as today and the main treatment was fresh air and sun, preferably close to the sea. After being used for other healthcare purposes and also appointed to "National interest for cultural heritage" in 1989, the sanatorium was in the 90's converted to an exclusive spa facility, hotel and conference.

Each year the SSoCC conference is given a specific theme. After having focused on Radio for a couple of years, this year it was time for the theme "Future CPU-centric electronic system". The four invited speakers, all from the area of digital design, presented different views on the theme from academia and industry, locally and internationally.

The keynote speaker was Professor Mladen Berekovic from Braunschweig University of Technology in Germany with his "Power-Efficient Processor Design for Future Systems-on-chip". He started by pointing out how our needs for computing power in mobile applications are growing significantly faster than the technology itself can supply the mobile power, at the same time as we expect improved power efficiency (energy efficiency) as most of the applications are battery powered. Moore's Law has helped us a lot but we can not forever rely on smaller geometries and faster transistors. Parallelism (multi-core processors) is used today to continue the increase in performance after the GHz-clock scaling hit the wall a couple of years ago. But soon, we will again be limited by power consumption. Perhaps the most important figure-of-merit is the power consumption per instruction. How can we improve it? There are a number of methods in the areas of circuit design and architectures that are well-known today. But what professor Berekovic particularly studied during his time at the research institute IMEC in Belgium is reconfigurability "on-the-fly". There is a general contradiction between

flexibility and efficiency, but by using an architecture that very rapidly is reconfigurable at different levels in the architecture, both flexibility and efficiency can be reached simultaneously. The architecture has been licensed by several companies. He continued his presentation by giving examples from commercially available solutions for flexible processors (e.g. Videantis, TI DaVinci, NXP EVP, Tensicila ASIP) and finally gave an overview of the EU research in the field.

Jiri Gaisler from Gothenburg-based Aeroflex Gaisler described how the LEON processor was developed for critical space purposes by the European Space Agency (ESA) and then released as open source. Today it is a part of a larger IP library, GRLIB, which can be implemented in both FPGAs and ASIC hardware. The processor is now in its fourth generation, used not only in the space (the design is insensitive to radiation) but also in consumer electronics, and in research and student projects due to its open nature.

From Atmel in Trondheim, Norway, came Development Director Frode Pedersen, and gave an insight into something that is everywhere but even electronics engineers and scientists often forget: the microcontroller. It is a very competitive product with short development times. It may be general or optimized for a particular application together with a customer. The key parameter is often low power and Frode Pedersen discussed a number of techniques to reduce the power consumption, such as by advanced sleep functions that can be tailored for each application.

In the last lecture, Dr. Ioannis Sourdis from Chalmers, led us back to a scientific approach to system-on-chip and reconfigurable hardware. Also Dr. Sourdis pointed out the limitations of technology scaling, but at the same time he was basically positive since the resources on the chip level are increasing constantly - the problem is to use them! FPGAs are interesting; they are very flexible (but can use large chip area) and there are applications where they can be several hundred times more powerful than a general processor (e.g. x86 architecture) that solves all problems in the software. As examples of research in this area, he described the recently started project DeSyRe in which Chalmers participates. By using a general framework for embedded system-on-chip, where the chip is partitioned into different blocks depending on requirements on processing/reliability margins, it is possible to make extremely flexible and inexpensive chip. The technology will demonstrated by designing an artificial pancreas on a chip, and the design of a chip to replace damaged parts of the cerebellum in the brain.

Each year there is a “Best Student Paper Award”. A winning entry must contain good scientific results, give a good oral presentation, and have submitted a well-written four-page paper to the conference. This year the price was divided into two parts; one for digital design and one for analog/RF design. Deepak Dasalukunte from Lund University won the award for best digital design paper with “Improved Memory Architecture for Multicarrier Faster-than-Nyquist Iterative Decoder” (coauthors Fredrik Rusuk and Viktor Öwall). Timmy Sundström from Linköping University won (for the second year in a row!) the price in the analog/RF category with the paper “A power efficient 1-GS/s single-channel pipeline ADC in 65nm CMOS utilizing analog gain trimming” (coauthors Christer Svensson and Atila Alvandpour).

Deepak Dasalukunte from Lund University with Prof. Lars Svensson

Timmy Sundström from Linköping University with Prof. Svante Signell.

Next year, the conference will be held in the Stockholm area with local support by the Royal Institute of Technology.

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